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(54) Organic substrate for flip chip bonding

(57) An exemplary embodiment of the present invention described and shown in the specification and drawings is a substrate (14) that has lattice points (118) and interstitial points (142). The substrate (14) includes a surface (24), a plurality pads (140) located on the surface at interstitial points (142), and a plurality of vias (120) located in the substrate only at lattice points (118).

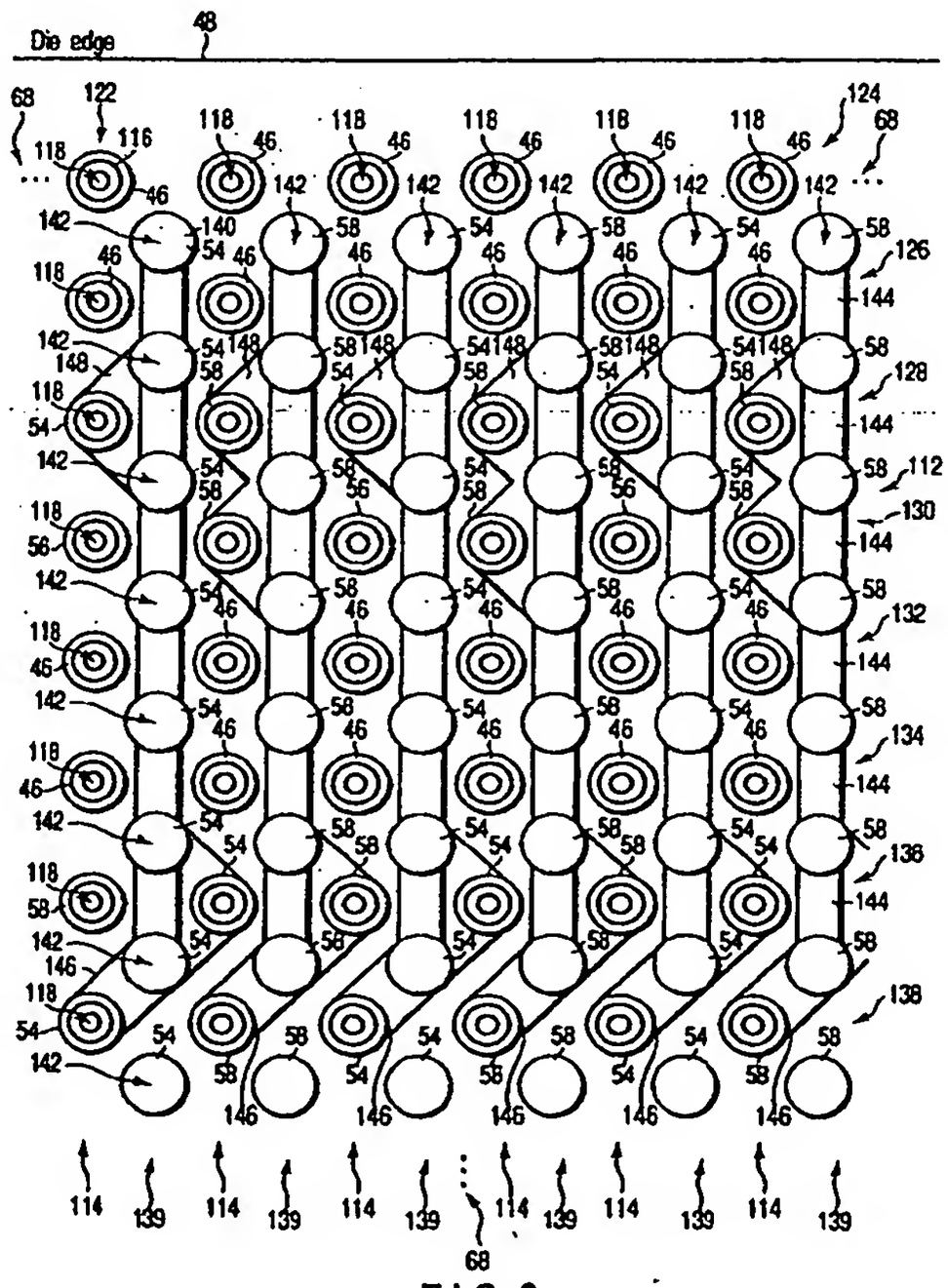

FIG. 9

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Description

[0001] The present invention relates to semiconductor packaging, and in particular, to an organic substrate for flip chip semiconductor packages.

[0002] Referring to FIGS. 1 and 2, a flip chip bonding configuration for a semiconductor package 10 that includes a semiconductor die 12 that is mechanically and electrically connected to a supporting substrate 14. Metallic bumps 16 on the bottom surface 18 of the die 12 overlap with metallic pads 20 correspondingly positioned in a die bonding region 22 located on the top surface 24 of the substrate 14. Typically, the metallic bumps 16 are connected to the underlying pads 20 by solder 26, thus providing direct electrical coupling between the die 12 and substrate 14. The direct electrical interconnection between the die 12 and substrate 14 provided by flip chip bonding configuration 10 advantageously eliminates the need for bond wires and results in low resistance and inductance values. Thus, flip chip bonding configurations provide for better signal integrity and power distribution to and from the die 12 than in other bonding technologies such as wire bonding or tape automated bonding.

[0003] The bottom surface 18 of the die 12 may include hundreds of metallic bumps 16 with each metallic bump providing an electrical interface to and from the die 12 for various electrical signals, core power, input/output (I/O) power, and ground. Electrical signals, core power, and ground are provided to the die's internal logic circuitry (not shown). Similarly, the I/O power and ground are provided to the die's I/O interface circuitry (not shown), i.e., input and output drivers. The metallic bumps 16, and therefore the corresponding pads 20 on the top surface 24 of the substrate 14, generally are arranged in concentric rectangular rings (not shown) and are spaced apart to prevent electrical shorting between adjacent metallic bumps/pads. However, the metallic bumps 16 and pads 20 may be configured in various patterns other than concentric rectangular rings.

[0004] The substrate 14 may be a multi-layer printed circuit board, ceramic substrate or another semiconductor chip. Typically, pads 28 on the bottom surface 30 of the substrate 14 are bonded, e.g., via solder 32, to another printed circuit board referred to as a motherboard 34. The substrate 14 provides for a mechanical and electrical interface between the often densely-packed metallic bumps 16 on the bottom surface 18 of the die 12 to less-densely packed pads (not shown) on the motherboard 34. The pads 28 on the substrate's bottom surface 30 are placed so as to correspond to the pads (not shown) on the motherboard 34.

[0005] The various layers of the substrate 14 are formed by the well known processes used to create integrated circuits and printed circuit boards. The individual layers may be comprised of conductive or semiconductor material. Often, the conductive material is a metal, i.e., a copper-based material, which is plated onto semiconductor material layers and patterned by photolithographically removing deposited metal to form pads and traces. The substrate 14 may be referred to as organic if organic material is combined with the copper-based material so as to provide thermal expansion characteristics close to those of the motherboard 34 and to improve reliability in board assembly.

[0006] Traces (not shown) electrically interconnect pads 20 or 28 on either the top surface 24 or bottom surface 30 of the substrate 14 or to vias (not shown) which are holes that facilitate the electrical interconnection of the various layers of the substrate 14. The vias may be formed, for example, by mechanical or laser drilling a via hole through a layer or layers of the substrate 14. Surrounding the via hole on each level may be a circular land (not shown) made of a conductive material. Typically, the via hole is filled with a conductive material so that via lands surrounding the via holes on various layers of the substrate are electrically interconnected. A via may extend through to the bottom surface 30 of the substrate 14 and connect to a pad 28. Thus, the pads 20 and 28 on the top surface 24 and bottom surface 30, respectively, of the substrate 14 are interconnected to one another by means of traces and vias. Solder balls 32 are individually connected to each pad 28 for soldering the pads 28 on the bottom surface 30 of the substrate 14 to the corresponding pads (not shown) on the motherboard 34. The solder balls 32 connected to the pads 28 on the bottom surface 30 of the substrate 14 are collectively called a ball grid array 36.

[0007] Various electrical characteristics are considered when designing the substrate 14 including maintaining a low DC resistance and AC inductance for power and ground connections to and from the die 12, and maintaining wide spacing between traces (not shown), pads 20 and 28, and via lands (not shown) to minimize the possibility of crosstalk or electrical shorting. Thus, with respect to power distribution for the die 12, the distance between the pads 20 on the top surface 24 of the substrate 14 for core power distribution and the logic circuitry which actually consume the power should be as short as possible.

[0008] Recently, many semiconductor packages have been designed using C4 flip chip bonding technology. An exemplary C4 bonding technology pad arrangement 38 is shown in the top plan view of FIG. 3. Referring additionally to FIGS. 1 and 2, the C4 bonding technology utilizes pads 40 arranged in an area array in the die bonding region 22 on the top surface 24 of the substrate 14 that are separated from one another by a pitch "p". In FIG. 3, the pads 40 are positioned at lattice points 41 (only numbered along one row and one column), where each lattice point 41 is located below the midpoint of each pad 40.

[0009] In FIG. 3, the top two rows 42 and 44 of pads 40 from adjacent the die edge are rows of signal pads 46 that accommodate the transfer of various electrical signals to and from the die 12. The top two rows 42 and

44 of pads 40 closest to the die edge 48 include signal pads 46 because the majority of the logic circuitry within the die 12 is located proximate to the die edge 48 and signal traces (not shown) on the top surface 24 of the substrate 14 are typically routed outside of the die bonding region 22. The third and fourth rows 50 and 52, respectively, of pads 40 down from the die edge 48 include core power pads 54, for the transfer of power to the logic circuitry in the die 12, I/O power pads 56, for the transfer of power to the I/O interfaces in the die 12, and ground pads 58, for providing ground connections to the die. The fifth and sixth rows 60 and 62, respectively, of pads 40 down from the die edge 48 are again rows of signal pads 46. The seventh and eighth rows 64 and 66, respectively, of pads 40 are core power pads 54 and ground pads 58. Thus, power and ground pads 54 and 58, respectively, are intermingled with the signal pads 46 so as to avoid problems that occur when large numbers of signal pads 46 result in the power and ground pads 54 and 58, respectively, being located further than three to four rows away from the die edge. The three dots 68 in the upper left hand corner, upper right hand corner, and the bottom of FIG. 3 indicate that the number and spacing between the pads 40 included in the pad arrangement 38 can vary along the top surface 24 of the substrate 14 in those directions.

[0010] FIG. 3 indicates examples of the maximum distances between the die edge 48, where the logic circuitry is assumed to be located, and a core power pad 54 and an I/O power pad 56. A maximum distance between the die edge and a core power pad is approximately 3.354p (3.354 times p), where p is the pitch or distance between the midpoints of adjacent pads 40. Also, a maximum distance between the die edge and an I/O power pad is approximately 4.272p (4.272 times p). If p is 0.25 millimeter, the distance between the die edge and the core power pad reaches approximately 0.8385 millimeter, and the distance between the die edge and the I/O power pad reaches approximately 1.068 millimeters. These distances may result in increased DC resistance and AC inductance values.

[0011] FIG. 4 is a top plan view of underlying layers of vias 70 that connect to the pads 40 in FIG. 3. Again, the vias 70 are used to rout electrical signals, core power, I/O power, and ground potential to the layers of the substrate 14 below the top surface 24. Each via 70 includes a via hole 72 indicated by the inside circle 73 with an accompanying ring-shaped via land 74 which surrounds the via hole 72 as indicated by the second concentric circle 75. The vias 70 in each underlying layer are located directly below the corresponding pads 40 at the lattice points 41 on the top surface 24 of the substrate 14, and thus, utilize a pad-on-via structure. Accordingly, the top two rows 76 and 78 of vias 70 adjacent the die edge 48 are rows of signal vias 80 that accommodate the transfer of various electrical signals. The third and fourth rows 82 and 84, respectively, of vias 70 down from the die edge 48 include core power vias 86, I/O power vias 88, and ground vias 90. The fifth and sixth rows 92 and 94, respectively, of vias 70 down from the die edge 48 are again rows of signal vias 80. The seventh and eighth rows 96 and 98, respectively, of vias 70 are core power vias 86 and ground vias 90. The three dots 68 in the upper left hand corner, upper right hand corner, and the bottom of FIG. 4 indicate that the number and spacing between the vias 70 included in the arrangement of vias 70 can vary along each layer in those directions.

[0012] FIG. 5 is a top plan view of another C4 bonding configuration pad arrangement 100, based upon the pad arrangement 38 of FIG. 3, in which additional core power pads 54 and additional ground pads 58 are alternatingly placed in columns of core power pads 102 and columns of ground pads 104 at the interstitial points 106 (only numbered along one row and one column), where each interstitial point 106 is the mid point between four adjacent lattice points 41. Similar to FIG. 3, FIG. 5 includes signal pads 46, core power pads 54, I/O power pads 56, and ground pads 58. The three dots 68 in the upper left hand corner, upper right hand corner, and the bottom of FIG. 5 indicate that the number and spacing between the pads 40 included in the pad arrangement 100 can vary along the top surface 24 of the substrate 14 in those directions. As shown in FIG. 5, a maximum distance between a core power pad 54 and the die's logic circuitry, presumably located proximate to the die edge 48, is only approximately 1.803p (1.803 times p). Therefore, if p equals 0.25 millimeter, the distance between the core power pad and the logic circuitry will be approximately 0.4508 millimeter. Thus, by adding core power pads 54 and ground pads 58 at the interstitial points 106, the pad arrangement 100 of FIG. 5 offers improved power distribution performance over the pad arrangement 38 of FIG. 3.

[0013] Similar to the C4 bonding configuration of FIGS. 3 and 4, the C4 bonding configuration of FIG. 5 utilizes a pad-on-via structure as shown in the top plan view of underlying layers provided by FIG. 6. Again, signal vias 80, core power vias 86, I/O power vias 88, and ground vias 90, respectively, are used to rout electrical signals, core power, I/O power, and ground potential to the layers of the substrate 14 below the top surface 24. The three dots 68 in the upper left hand corner, upper right hand corner, and the bottom of FIG. 6 indicate that the number a spacing between the vias included in the via arrangement can vary along each layer in those directions. One problem associated with the C4 bonding configuration shown in FIG. 6, is that the minimum pitch between adjacent vias is only approximately 0.707p (0.707 times p), or approximately 0.1767 millimeters when p equals 0.25 millimeter. This is a smaller pitch between vias than that of the C4 bonding configuration of FIG. 4. The reduced via pitch is of concern when routing traces (not shown) between vias as discussed below.

[0014] Process design rules are used during semi-

conductor packaging design to limit the placement of adjacent metallic regions relative to one another, and thus, ensure that short circuits and/or open circuits do not occur in semiconductor devices. Process design rule values are determined, at least in part, based upon inherent limitations in the precision of the photolithography and/or etching techniques used when forming the metallic layers of the substrate 14. FIG. 7 is a magnified top plan view of two signal traces 108 routed between two adjacent vias 70 for the C4 bonding configuration of FIGS. 3 and 4. As shown in FIG. 7, if the diameter of the via land 74 is approximately 0.11 millimeter, and the process design rule is 28 micrometers, the two traces 108 having a 28 micrometer trace width can be routed between the vias 70 leaving a 28 micrometer space between adjacent metal.

[0015] FIG. 8 is a magnified top plan view of a signal trace 110 routed between two adjacent vias 70 for the C4 bonding technology configuration of FIGS. 5 and 6. In contrast to FIG. 7, only one trace 110 can be routed between the vias 70. Also, a finer design spacing value of approximately 22 micrometers, instead of 28 micrometers, is required in FIG. 8. Therefore, if the C4 bonding configuration of FIGS. 5, 6, and 8 is to be used, more layers and a finer design spacing rule is required, both of which increase the overall cost for the substrate 14. Thus, there is a need to reduce the distance between the core power pads 54 and the die's logic circuitry without increasing the overall cost of the substrate by requiring more layers and finer design spacing rules.

[0016] In one aspect of the present invention, a substrate has lattice points and interstitial points. The substrate includes a surface, a plurality of pads located on the surface at the lattice points and the interstitial points, and a plurality of vias formed in the substrate to be located at the lattice points and not located at at least one of the interstitial points.

[0017] In another aspect of the present invention, a semiconductor package includes semiconductor die that has a die edge and a substrate connected to the semiconductor die that has lattice points and interstitial points. The substrate includes a surface, a plurality of pads located on the surface at the lattice points and the interstitial points, and a plurality of vias formed in the substrate to be located at the lattice points and not located at at least one of the interstitial points.

[0018] In another aspect of the present invention, a method is disclosed for configuring vias in a substrate that has lattice points and interstitial points and for configuring pads on the surface of the substrate. The method includes locating pads on the surface of the substrate at interstitial points, and locating vias in the substrate only at lattice points.

[0019] It is understood that other aspects of the present invention will become readily apparent to those skilled in the art from the following detailed description, wherein is shown and described only exemplary embodiments of the invention, simply by way of illustration of the best mode contemplated for carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

[0020] Various features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings where:

FIG. 1 is a perspective view of a conventional flip chip bonding configuration;
FIG. 2 is a side plan view of a die soldered to a substrate;
FIG. 3 is a top plan view of a prior art pad arrangement in which the pads are located at the lattice points;
FIG. 4 is a top plan view of a prior art via arrangement in which the vias are located at the lattice points;
FIG. 5 is a top plan view of a prior art pad arrangement in which pads are located both the lattice points and the interstitial points;
FIG. 6 is a top plan view of a prior art via arrangement in which the vias are located at both the lattice points and interstitial points;
FIG. 7 is a top plan view of two vias and two traces in accordance with the via arrangement of FIG. 4;
FIG. 8 is a top plan view of two vias and a trace in accordance with the via arrangement of FIG. 6;
FIG. 9 is a top plan view of a pad arrangement in accordance with an exemplary embodiment of the present invention; and
FIG. 10 is a top plan view of a via arrangement in accordance with an exemplary embodiment of the present invention.

[0021] FIG. 9 is a top plan view of a top surface 24 of a substrate 14 in a die bonding region 22 and FIG. 10 is a corresponding underlying via layer of one exemplary embodiment of the present invention. FIG. 9 shows vertical columns 114 of pads 116 located at lattice points 118 (only numbered along one row and one column). The pads 116 located at the lattice points are electrically connected to vias 120 also located at lattice points 118 (only numbered along one row and one column) that pass through lower layers of the substrate 14 as shown in FIG. 10. These pads 116 that overly the vias 120 are referred to as "pad-on-vias" and are indicated by three concentric circles 122. Pads 140 without underlying vias 120 are located at the interstitial points 142 (only numbered along one row and one column) and are merely indicated by a single circle.

[0022] In the exemplary embodiment of FIG. 9, the top two rows 124 and 126 of pad-on-vias 116 from the die edge 48 are rows of signal pads 46 that accommodate

the transfer of various electrical signals to and from the die 12. The third and fourth rows 128 and 130, respectively, of pad-on-vias 116 down from the die edge 48 include core power pads 54, for the transfer of power to the logic circuitry in the die 12, I/O power pads 56, for the transfer of power to the I/O interfaces in the die 12, and ground pads 58, for providing ground connections to the die 12. The fifth and sixth rows 132 and 134, respectively, of pad-on-vias 116 down from the die edge 48 are again rows of signal pads 46. The seventh and eighth rows 136 and 138, respectively, of pad-on-vias 116 are core power pads 54 and ground pads 58.

[0023] The pad arrangement 112 of FIG. 9 also includes vertical columns 139 of pads 140 without underlying vias 120 which are located at the interstitial points 142 (only numbered along one row and one column) and may be core power pads 54 or ground pads 58. Some of the pads 140 without underlying vias 120 are electrically interconnected by wide traces 144 as shown in FIG. 9. Also, some of the pads 140 without underlying vias 120 are electrically interconnected to the pad-on-vias 116 by means of either wide traces 146 or triangular-shaped metallic layers 148. This arrangement, allows for core power and ground to pass through the vias 120 to the underlying layers of the substrate 14. The three dots 68 in the upper left hand corner, upper right hand corner, and the bottom of FIG. 9 indicate that the number and spacing between the pads 116 included in the pad arrangement 112 can vary along the top surface 24 of the substrate 14 in those directions.

[0024] Referring additionally to FIG. 10, located below the top surface 24 of the substrate 14 are vias 120 positioned in a via arrangement 149 under the lattice points 118 (only numbered along one row and one column) where the pad-on-vias 116 are located. Again, the vias 120 which are located at lattice points 118 are used to rout electrical signals, core power, I/O power, and ground potential to the layers of the substrate 14 below the top surface 24. Each via hole 72 is indicated by the inside circle 73 with an accompanying ring-shaped via land 74 which surrounds the via hole 72 as indicated by the second concentric circle 75. In the exemplary embodiment of FIG. 10, the top two rows 150 and 152 of vias from the die edge 48 are rows of signal vias 80 that accommodate the transfer of various electrical signals. The third and fourth rows 154 and 156, respectively, of vias down from the die edge include core power vias 86, I/O power vias 88, and ground vias 90. The fifth and sixth rows 158 and 160, respectively, of vias 120 down from the die edge are again rows of signal vias 80. The seventh and eighth rows 162 and 164, respectively, of vias 120 are core power vias 86 and ground vias 90. The three dots 68 in the upper left hand corner, upper right hand corner, and the bottom of FIG. 10 indicate that the number and spacing between the vias 120 included in the via arrangement 149 can vary along each layer in those directions.

[0025] Referring additionally to FIGS. 1 and 2, in operation, a die 12 is mechanically connected to the top surface 24 of the substrate 14, for example, by soldering metal bumps (not shown) on the bottom surface 18 of the die 12 to pads 20 located on the top surface 24 of the substrate 14 in the die bonding region 22. The bottom surface 30 of the substrate 14 may be mechanically connected to a motherboard 34, for example, by soldering pads 28 on the bottom surface 30 of the substrate 14 to pads (not shown) on the motherboard 34. Since the die 12, substrate 14, and motherboard 34 are electrically interconnected, electrical signals, core power, I/O power, and ground can be electrically coupled through the substrate 14, by means of the pads 20 and 28, respectively, on both the substrate's top surface 24 and bottom surface 30, and the substrate's vias 120, to and from the die's internal circuitry, i.e., logic circuitry and I/O circuitry.

[0026] The present invention advantageously offers a reduction in the distance between core power, I/O power, and ground pads 54, 56, and 58, respectively, and the logic circuitry located near the die edge 48. Embodiments of the present invention also maintain the via spacing of FIGS. 4 and 7, thus, allowing for at least two traces 108 to be routed between adjacent via lands 74 and eliminating the need for additional layers and narrower design spacing, both of which increase the overall cost of the substrate 14. In addition, the present invention provides wide traces 144 for core power and ground distribution which reduce DC resistance and AC inductance. Thus, the present invention provides improved performance over the C4 bonding pad and via configurations of FIGS. 3-8. Therefore, the present invention provides improved power distribution while maintaining conventional design spacing conventions.

[0027] Although exemplary embodiments of the present invention have been described, they should not be construed to limit the scope of the appended claims. Those skilled in the art will understand that various modifications may be made to the described embodiments. Moreover, to those skilled in the various arts, the invention itself herein will suggest solutions to other tasks and adaptations for other applications. It is therefore desired that the present embodiments be considered in all respects as illustrative and not restrictive, reference being made to the appended claims rather than the foregoing description to indicate the scope of the invention.

Claims

1. A substrate (14), having lattice points (18) and interstitial points (142), **characterized by** comprising:

   a surface (24);
   a plurality of pads (140) located on the surface at the lattice points and the interstitial points; and
   a plurality of vias (120) formed in the substrate

to be located at the lattice points and not located at at least one of the interstitial points.

2. The substrate according to claim 1, **characterized in that** the substrate (14) is for interconnecting to a semiconductor die (12) having a die edge (48) and the plurality of pads (140) are located on the surface at interstitial points (142) adjacent the die edge.

3. The substrate according to claim 2, **characterized by** further comprising at least one signal pad (46), for electrically coupling an electrical signal in and out of the semiconductor die (12), located on the surface at a lattice point (118) closer to the die edge (48) than the interstitial points (142).

4. The substrate according to claim 1, **characterized in that** each via (120) is electrically coupled to a pad (116) located at a lattice point (118).

5. The substrate according to claim 1, **characterized in that** the pads (140) located at the interstitial points (142) are core power pads (54) or ground pads (58).

6. The substrate according to claim 5, **characterized in that** at least one core power pad (54) located at an interstitial point (142) is electrically coupled to a pad (116) located at a lattice point (118).

7. The substrate according to claim 5, **characterized in that** at least one ground pad (58) located at an interstitial point (142) is electrically coupled to a pad (116) located at a lattice point (118).

8. The substrate according to claim 5, **characterized in that** at least one core power pad (54) located at an interstitial point (142) is electrically coupled to another core power pad (54) located at an interstitial point (142) by a trace (144).

9. The substrate according to claim 5, **characterized in that** at least one ground pad (58) located at an interstitial point (142) is electrically coupled to another ground pad (58) located at an interstitial point (142) by a trace (144).

10. The substrate according to claim 1, **characterized by** further comprising at least two signal traces (108) are routed between adjacent vias (70).

11. A semiconductor package **characterized by** comprising:

a semiconductor die (12) having a die edge (48); and
a substrate (14), having lattice points (118) and interstitial points (142), connected to the semiconductor die, the substrate including;
a surface (24) ;
a plurality of pads (140) located on the surface at the lattice points and the interstitial points; and
a plurality of vias (120) formed in the substrate to be located at the lattice points and not located at at least one of the interstitial points.

12. The semiconductor package according to claim 11, **characterized in that** the plurality of pads (140) are located on the surface at interstitial points (142) adjacent the die edge (48).

13. The semiconductor package according to claim 11, **characterized by** further comprising at least one signal pad (46), for electrically coupling an electrical signal in and out of the semiconductor die (12), located on the surface at a lattice point (118) closer to the die edge (48) than the interstitial points (142).

14. The semiconductor package according to claim 11, **characterized in that** the pads (140) located at the interstitial points (142) are core power pads (54) or ground pads (58).

15. The semiconductor package according to claim 14, **characterized in that** at least one core power pad (54) located at an interstitial point (142) is electrically coupled to a pad (116) located at a lattice point (118).

16. The semiconductor package according to claim 14, **characterized in that** at least one ground pad (58) located at an interstitial point (142) is electrically coupled to a pad (116) located at a lattice point (118).

17. The semiconductor package according to claim 14, **characterized in that** at least one core power pad (54) located at an interstitial point (142) is electrically coupled to another core power pad (54) located at an interstitial point (142) by a trace (144).

18. The semiconductor package according to claim 14, **characterized in that** at least one ground pad (58) located at an interstitial point (142) is electrically coupled to another ground pad (58) located at an interstitial point (142) by a trace (144).

19. The semiconductor package according to claim 11, **characterized by** further comprising at least two signal traces (108) are routed between adjacent vias (70).

20. The substrate according to claim 1, **characterized in that** no vias (120) are formed at the interstitial points (142) in the substrate (14).

21. The semiconductor package according to claim 11, **characterized in that** no vias (120) are formed at the interstitial points (142) in the substrate (14).

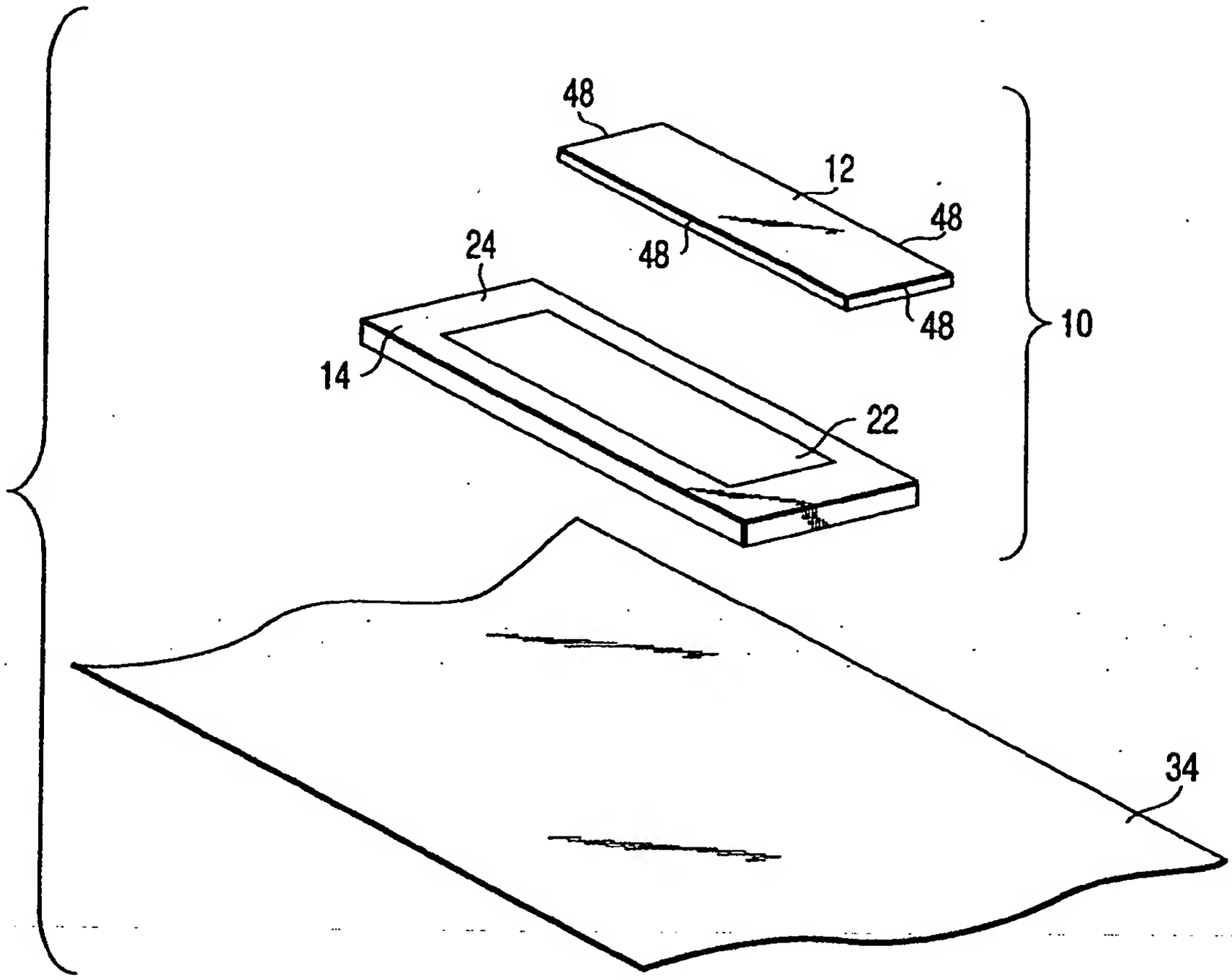


FIG. 1

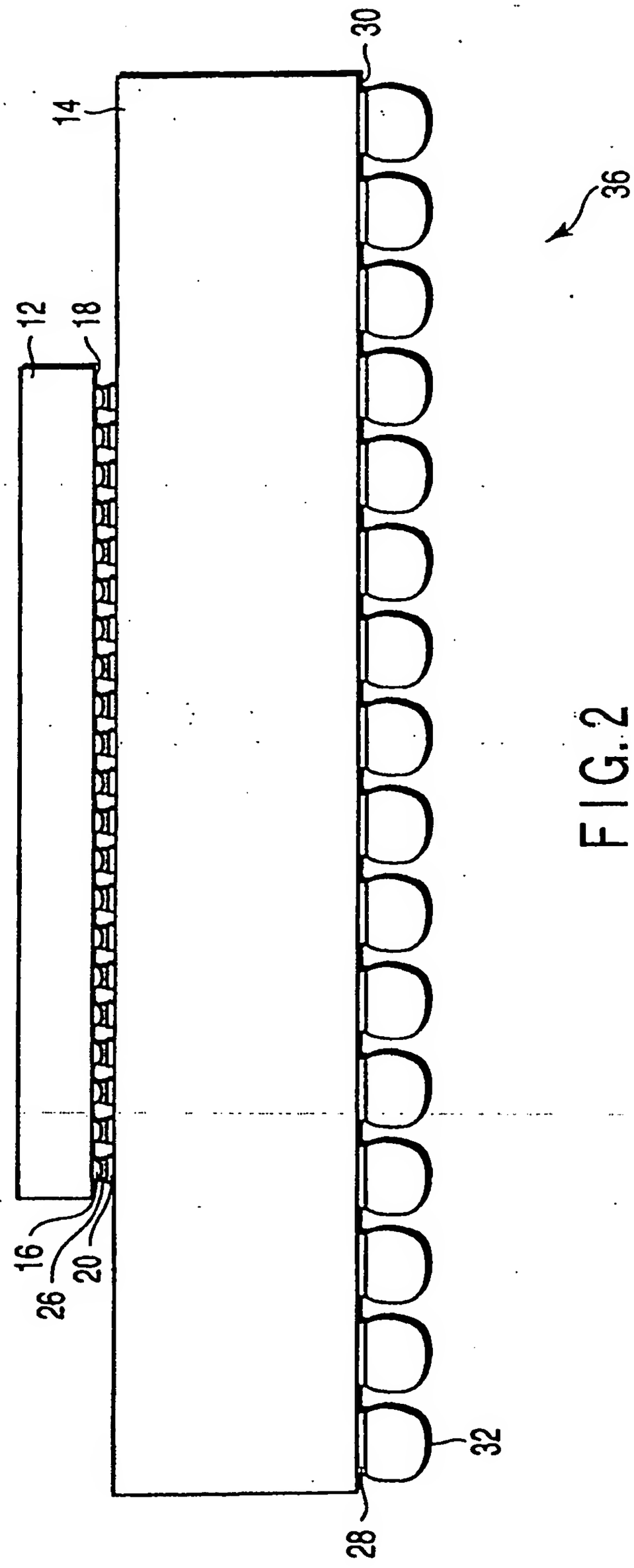
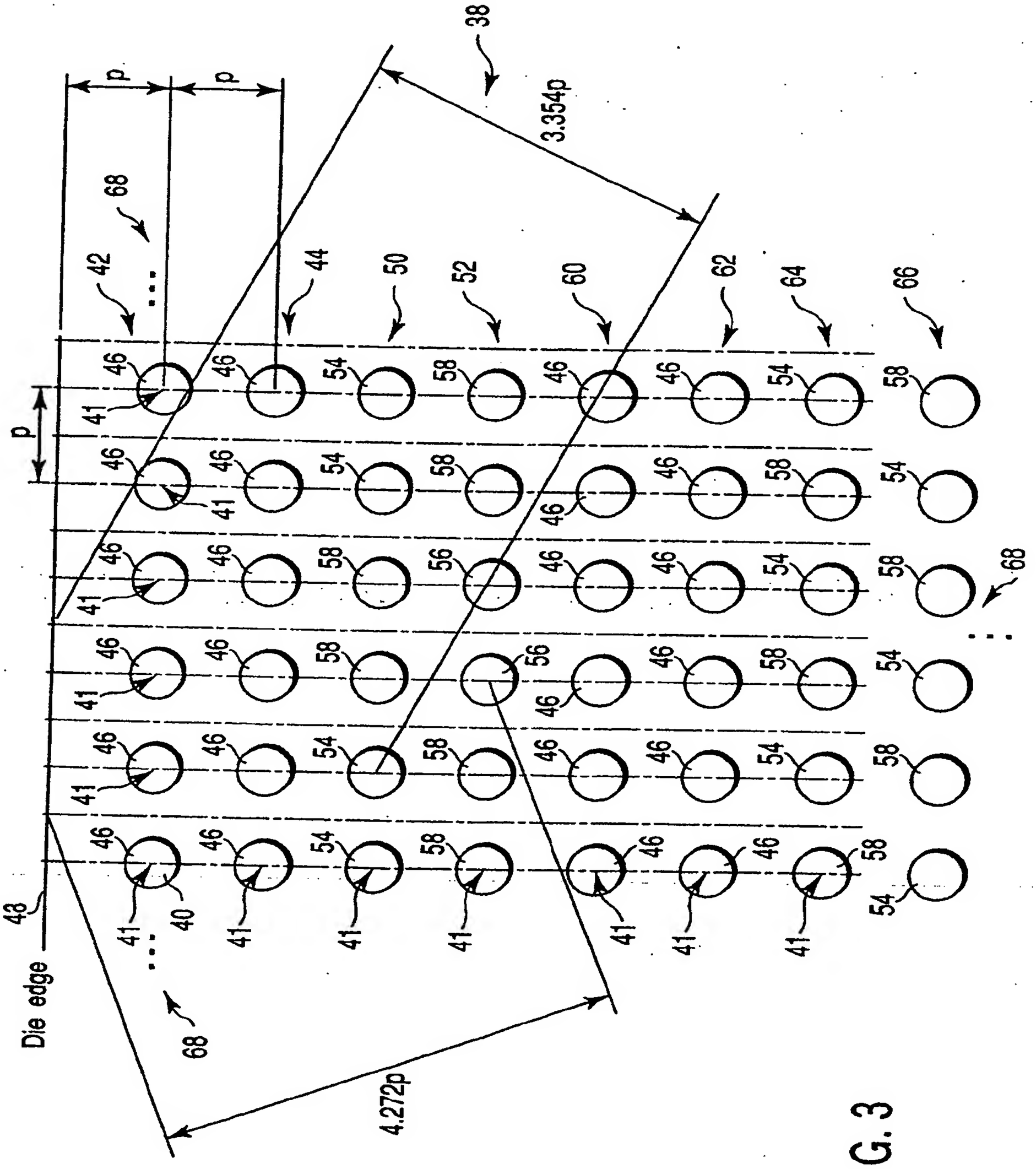


FIG.2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p
38
3.354p
68
42
44
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64
66
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41
54
58
56
40
43
Die edge
68
4.272p

FIG.3

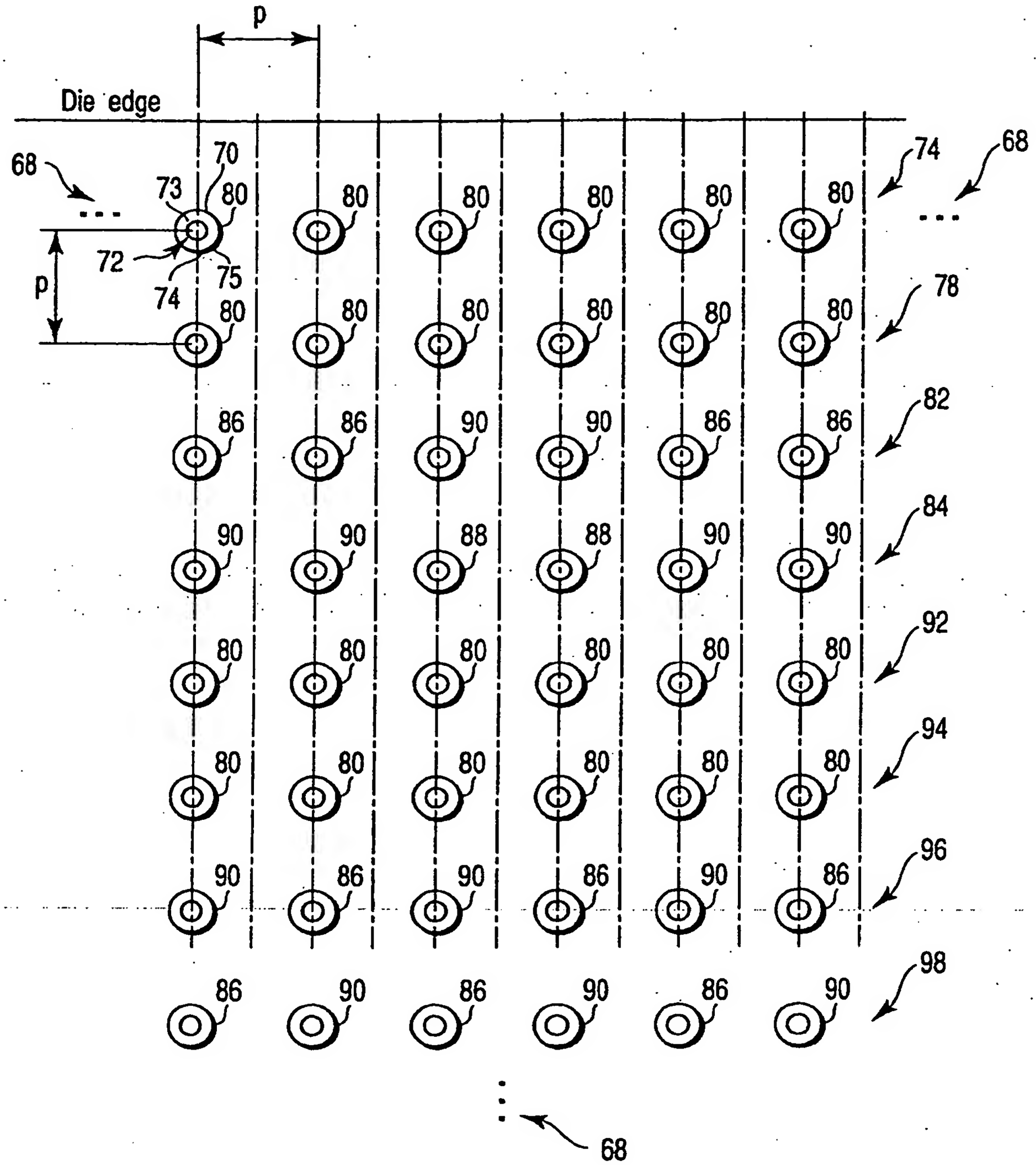


FIG. 4

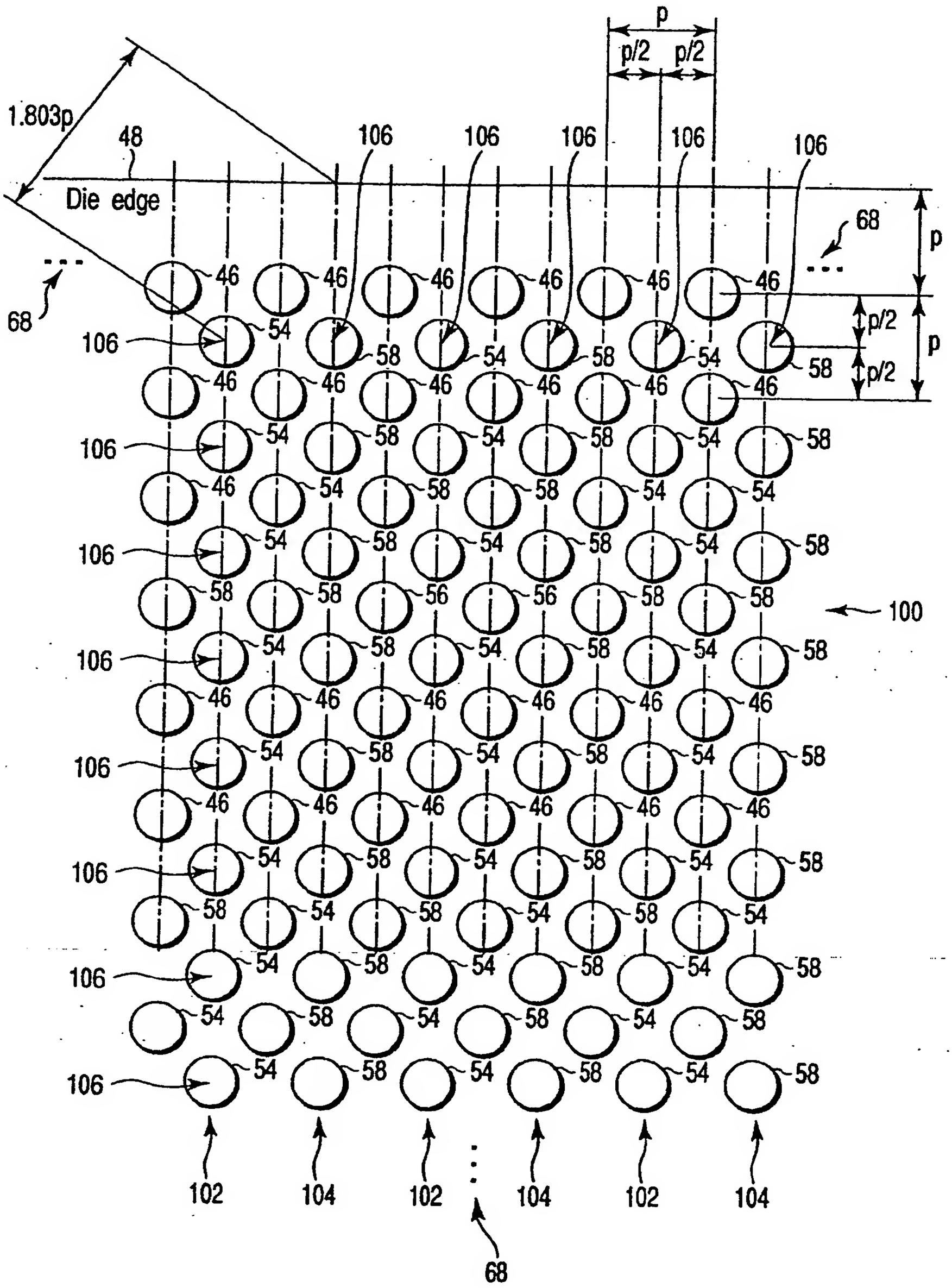


FIG.5

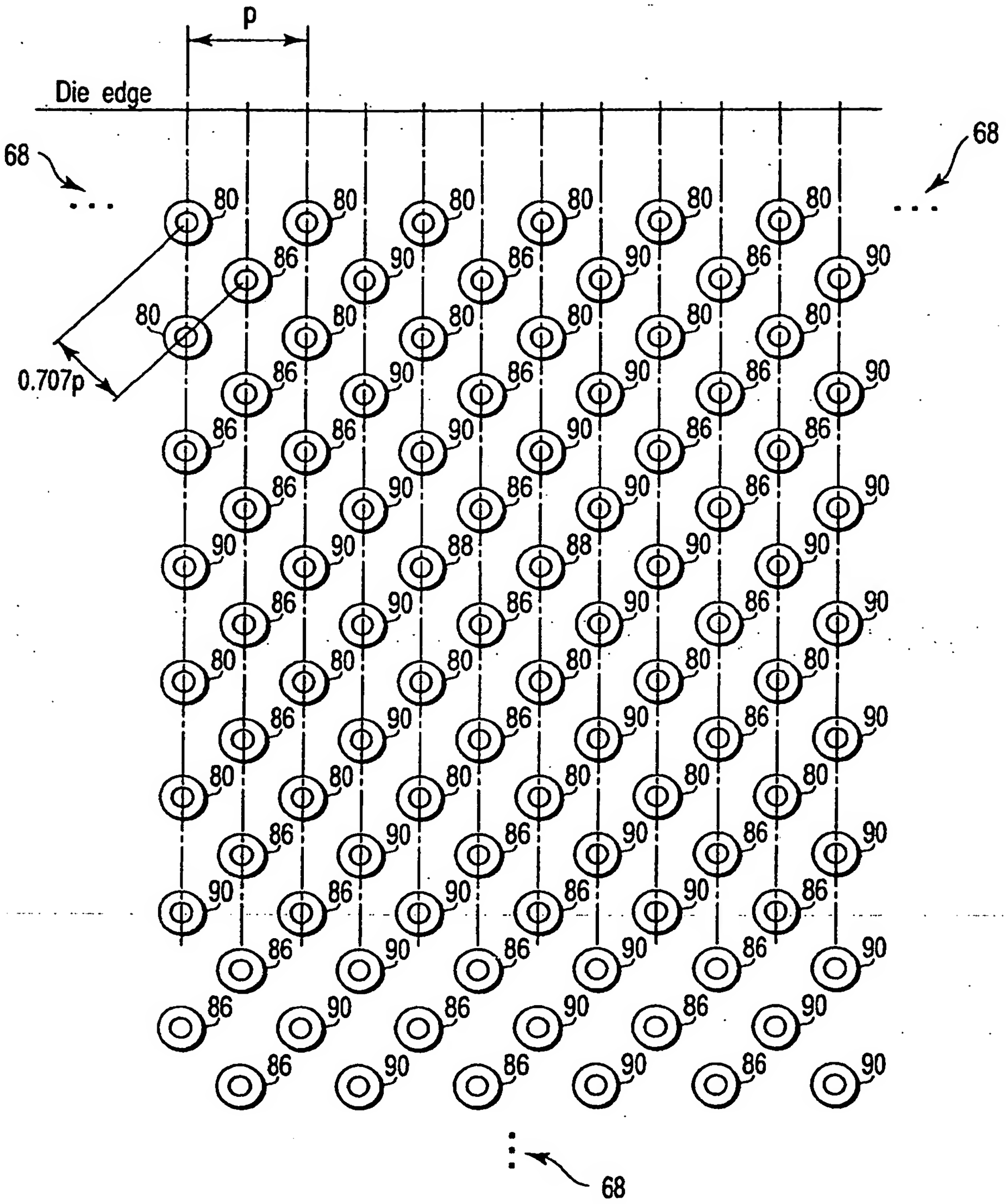
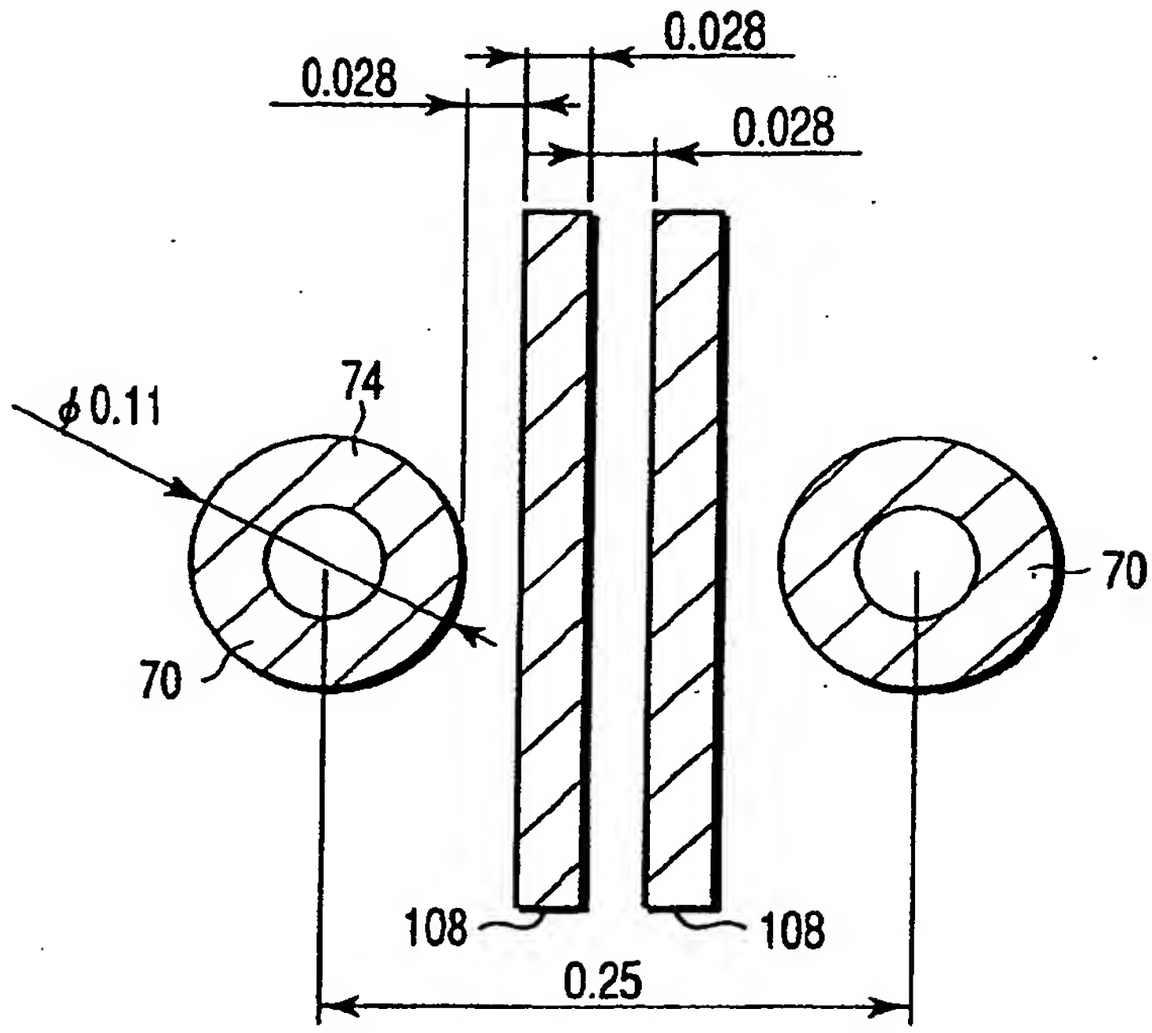


FIG.6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108
0.25

FIG. 7

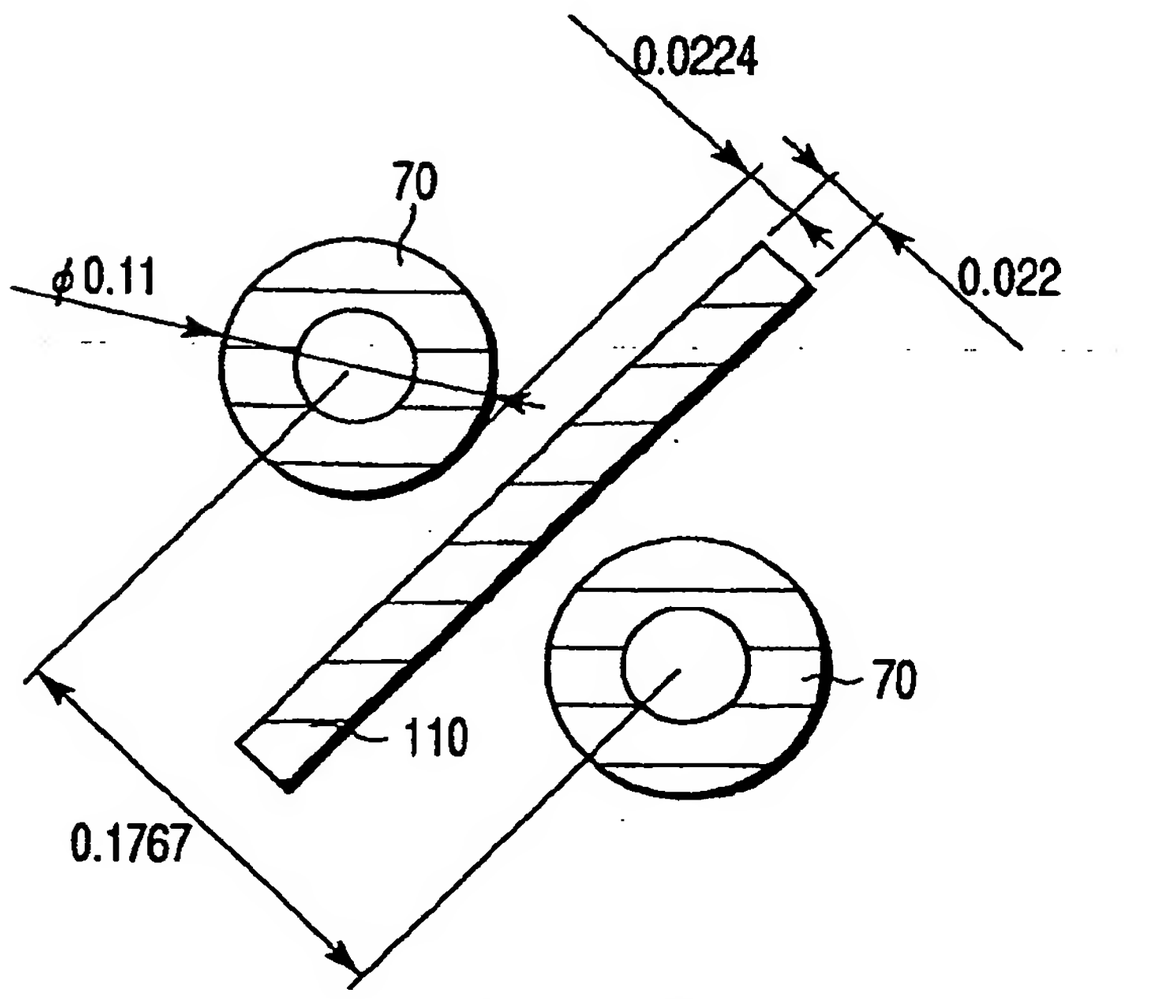
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FIG. 8

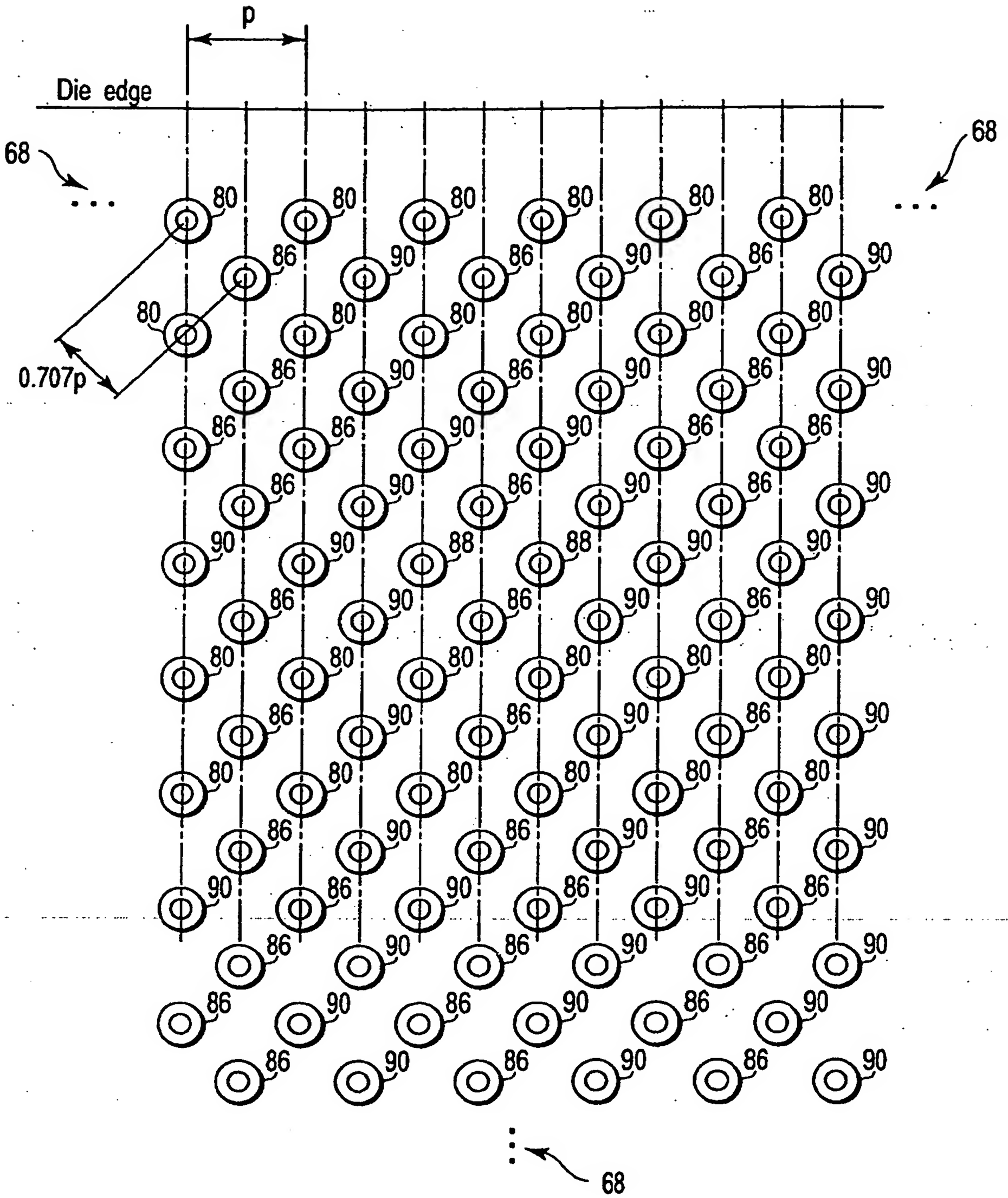

FIG.6

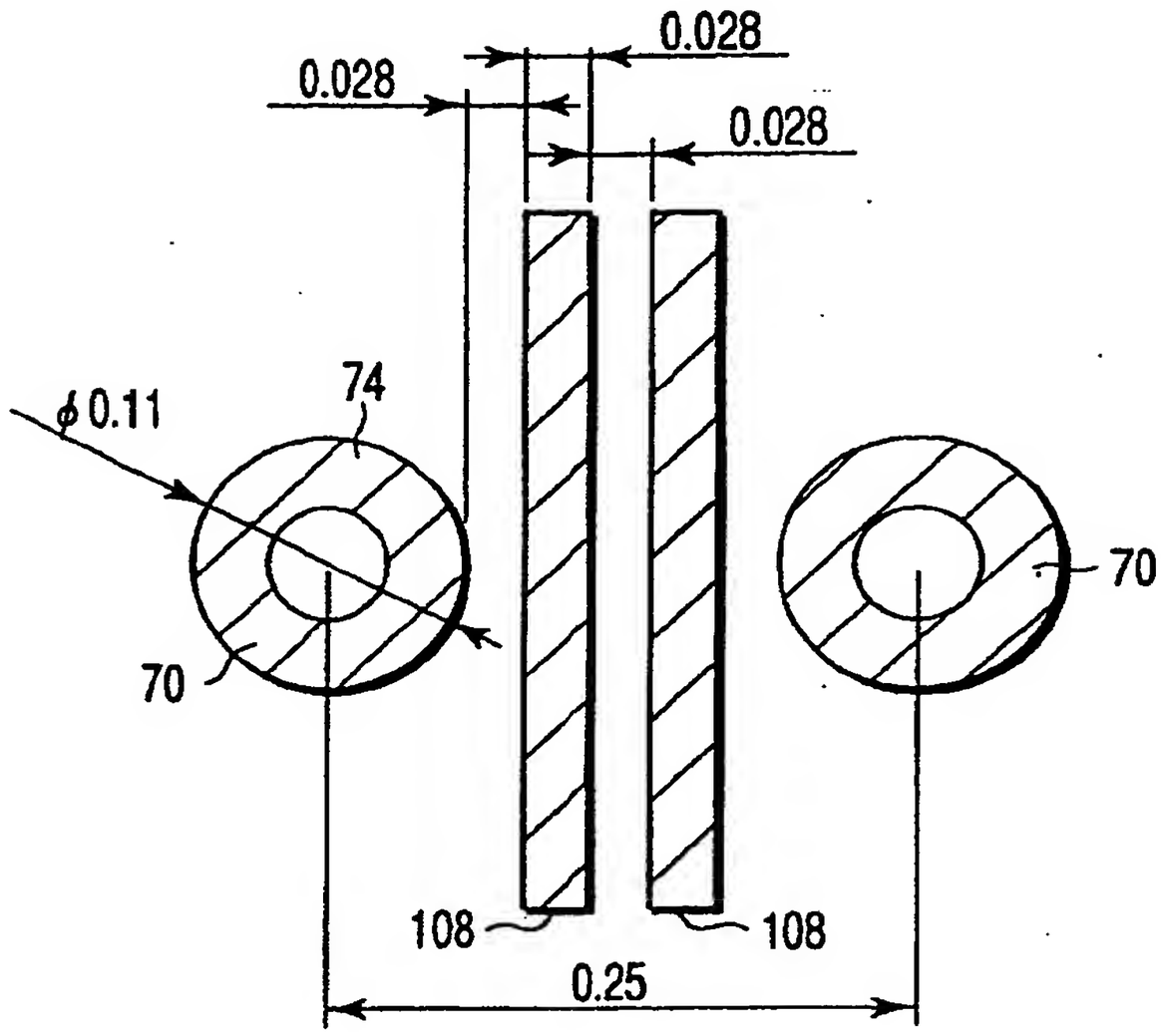

FIG. 7

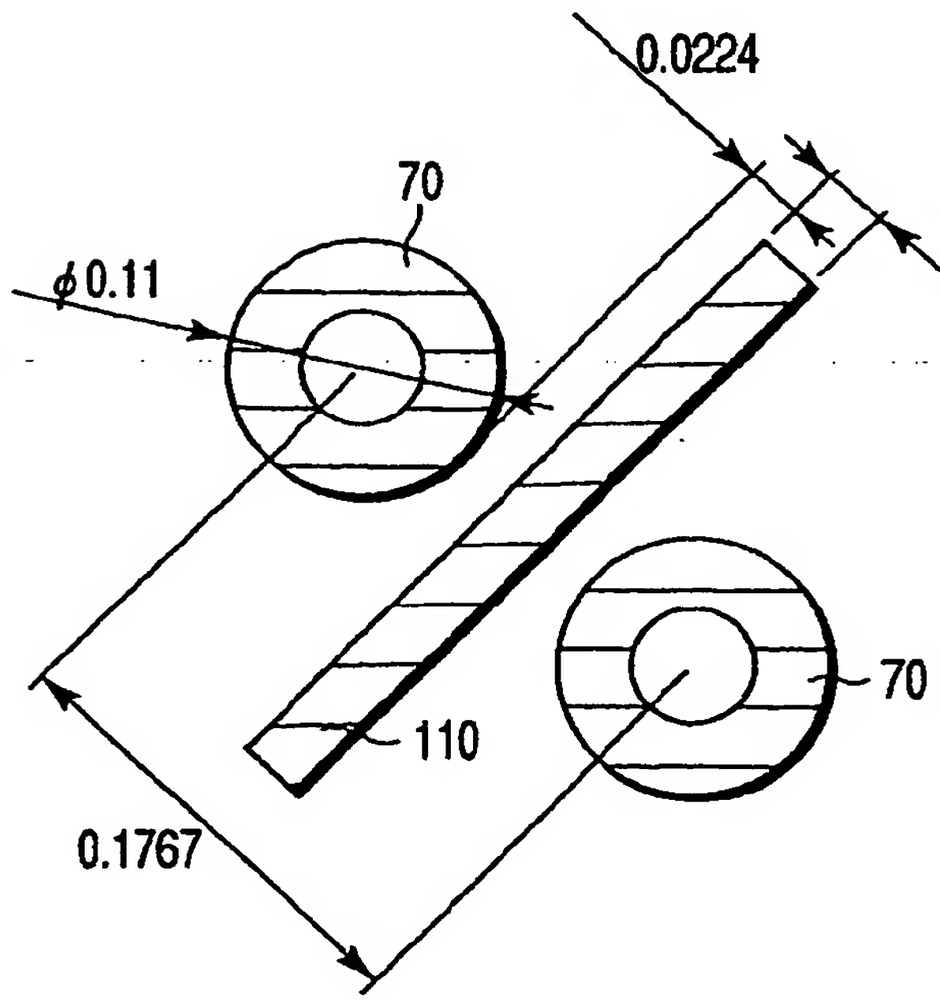

FIG. 8

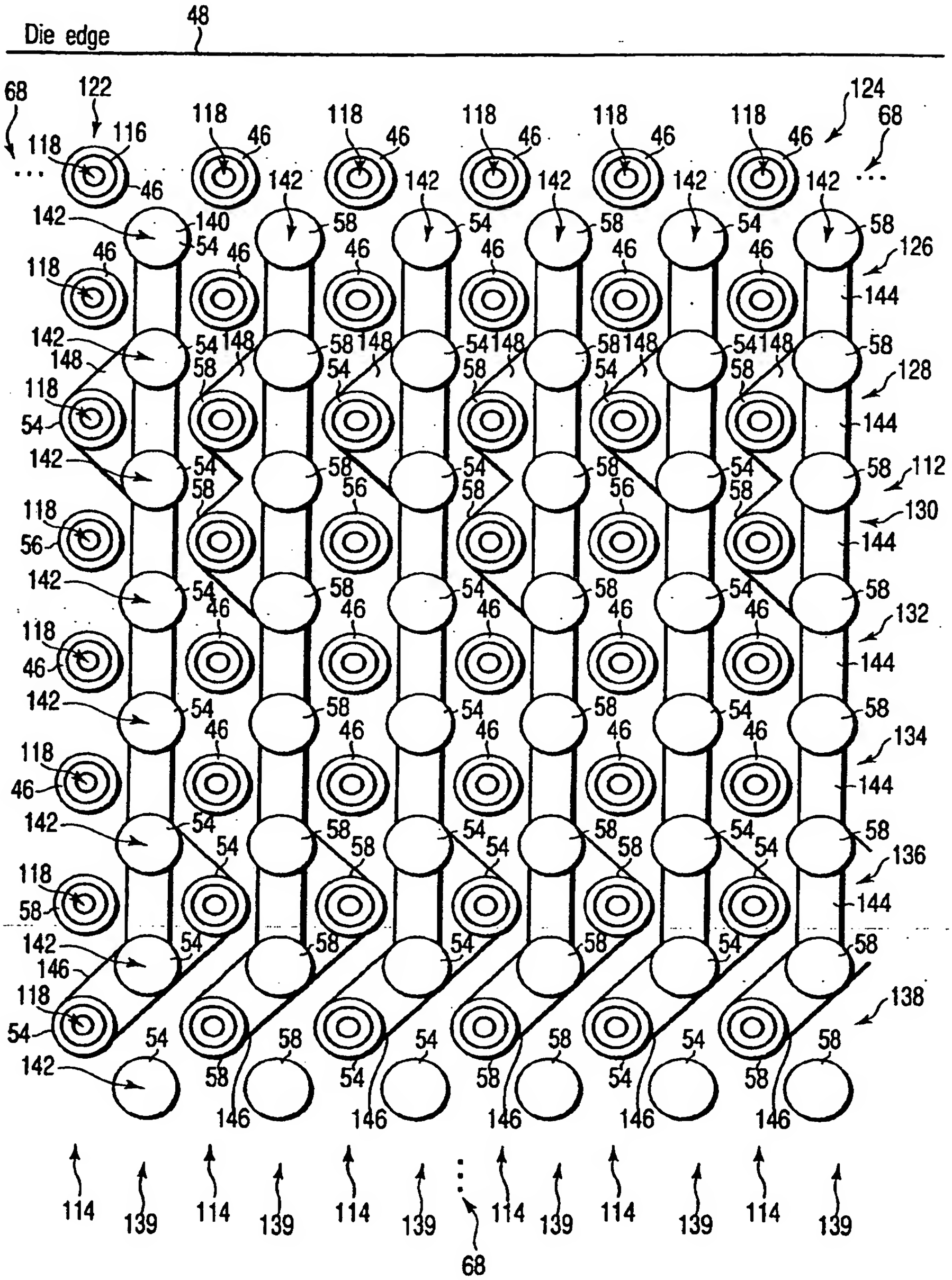

FIG. 9

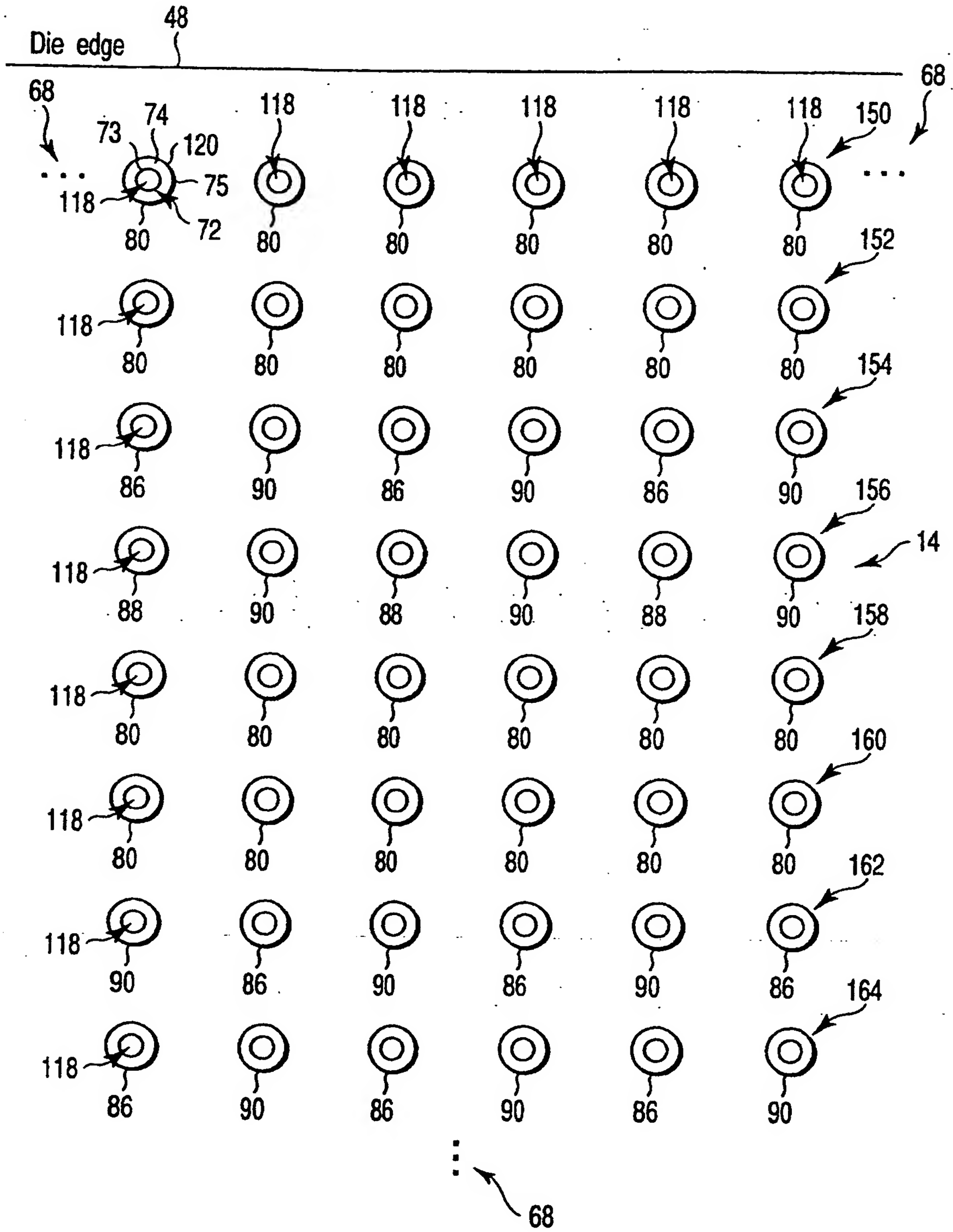

FIG. 10

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Arabellastrasse 4
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(54) Organic substrate for flip chip bonding

(57) An exemplary embodiment of the present invention described and shown in the specification and drawings is a substrate (14) that has lattice points (118) and interstitial points (142). The substrate (14) includes a surface (24), a plurality pads (140) located on the surface at interstitial points (142), and a plurality of vias (120) located in the substrate only at lattice points (118).

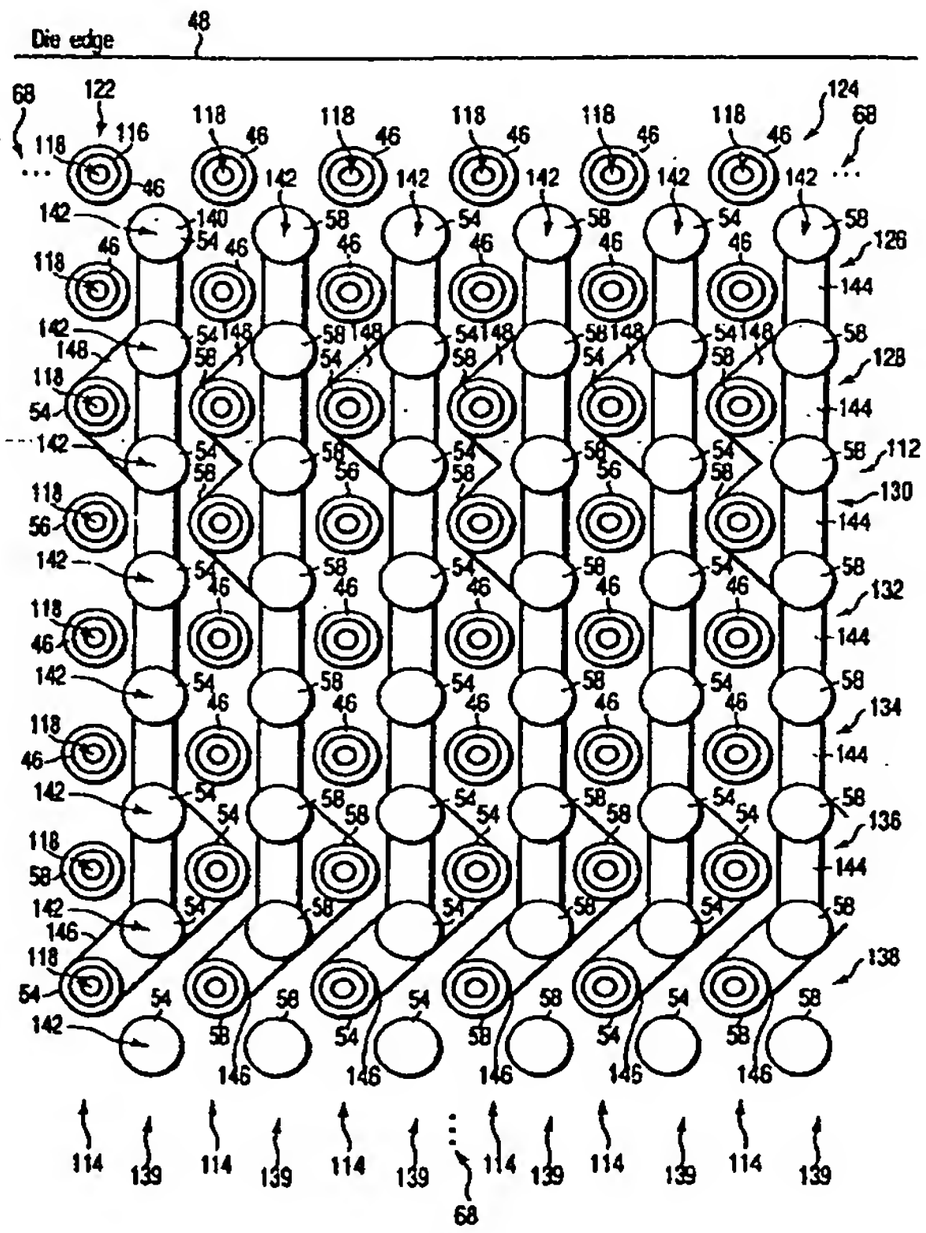

FIG. 9

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Application Number
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	27 March 2006	Hofer, C

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